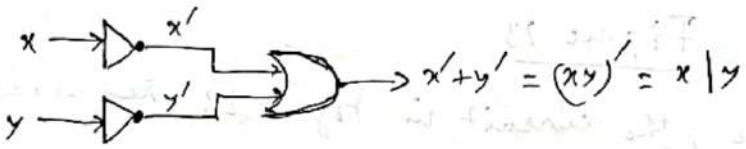
As we can see, the circuit in Figure 21 requires two gates. However we can draw the same circuit using only one NAND gate. Again by De Morgan's law $(xy)' = x' + y'$. To construct a logic circuit for $x' + y'$ we first negate both the inputs x and y and then feed the outputs through an OR gate.

Thus another equivalent circuit for a NAND gate is



Notice that this circuit contains three gates. We can replace the circuit by one NAND gate. Thus, we find that in the minimization problem the NAND gate plays a very useful role.

Next we describe the NOR gate

The symbol that is used for the Boolean expression $(x+y)'$ is called a NOR gate

The diagram in Figure 22 represents the NOR gate

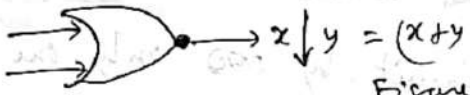


Figure - 22

The input-output table for the NOR gate is

NOR gate	input x	input y	output for NOR gate
	1	1	0
	1	0	0
	0	1	0
	0	0	1

In Boolean algebra, the expression $(x+y)'$ is also denoted by $x \downarrow y$. The binary operation symbol $\downarrow$ used in $x \downarrow y$ is called the Peirce arrow.

If we draw the circuit for the Boolean expression $(x+y)'$ using NOT and OR gates, then we obtain the circuit shown in Figure 23.

Figure 23

As we can see, the circuit in Figure 23 requires two gates. However, we can draw the same circuit using only one NOR gate. Again, by De Morgan's Laws, $(x+y)' = x'y'$. To construct a logic circuit for $x'y'$, we first negate both the inputs x and y and then feed the outputs through an AND gate. Thus another equivalent circuit for a NOR gate is

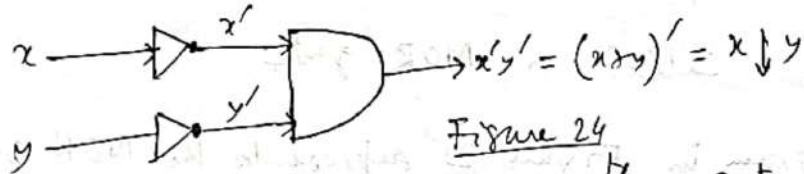


Figure 24

Notice that this circuit contains three gates. We can replace this circuit by "only one NOR gate. Thus, in the minimization problem the NOR gate also plays a useful role.

Worked out Examples

1. Construct a logic circuit corresponding to the Boolean expression $x(y'+z)+y$

Solution: We first negate the input y and feed the output y' and the input z through an OR gate. Then we feed the output of the OR gate, namely, y'+z, and the input x through an AND gate. Finally we feed the output of the AND gate and the input y through an OR gate to get the required logic circuit. The circuit is

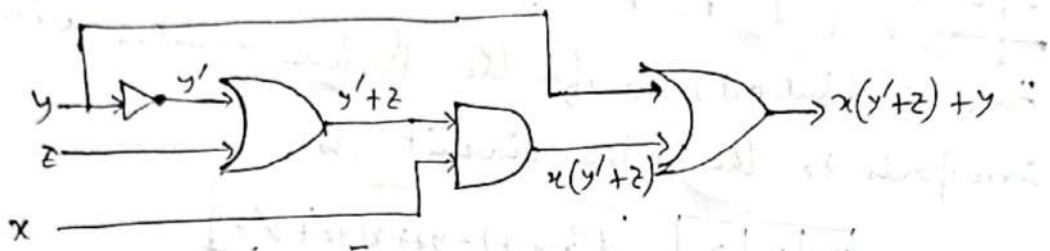
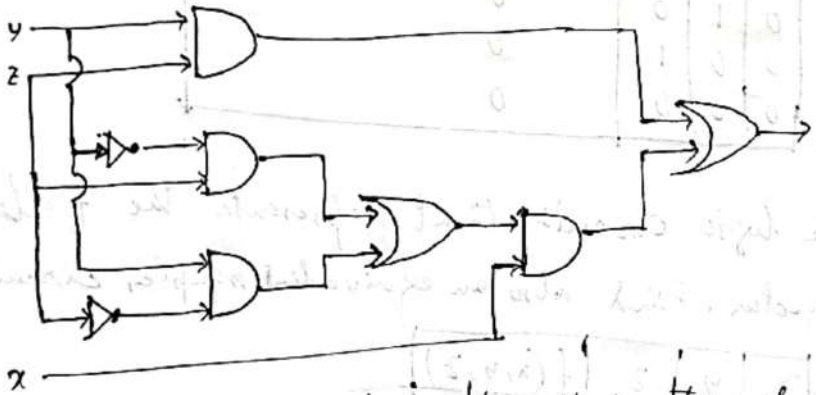


Figure 25

2. Write down the Boolean expression that represents the following logic circuit and then write down the input-output table.



Solution: First we write down the outputs through each gate. The required Boolean expression would be the output through the last gate of the circuit

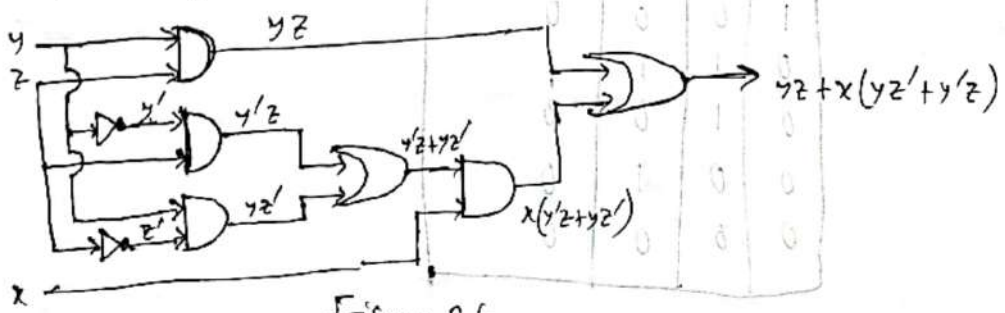


Figure 26

Hence the Boolean expression representing the given logic circuit is $yz + x(yz' + y'z)$

Its input-output table is the following:

x	y	z	y'	z'	yz'	y'z	yz'+y'z	x(yz'+y'z)	yz	yz + x(yz'+y'z)
1	1	1	0	0	0	0	0	0	1	1
1	1	0	0	1	1	0	1	1	0	1
1	0	1	1	0	0	1	1	1	0	1
1	0	0	1	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	1	1
0	1	0	0	1	0	1	1	0	0	0
0	0	1	1	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0	0	0	0

Hence the input-out table for the Boolean function which corresponds to the given circuit is

x	y	z	$f(x,y,z) = yz + x(yz' + y'z)$
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

3. Find the logic circuit that represents the following Boolean function. Find also an equivalent simpler circuit.

x	y	z	f(x,y,z)
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0