

University of Calcutta

Semester 4

PHYSICS

Paper: PHS-A-CC-4-10-TH (OLD SYLLABUS)

FIELD EFFECT TRANSISTOR

SOLVED PROBLEMS

ASSIGNMENTS

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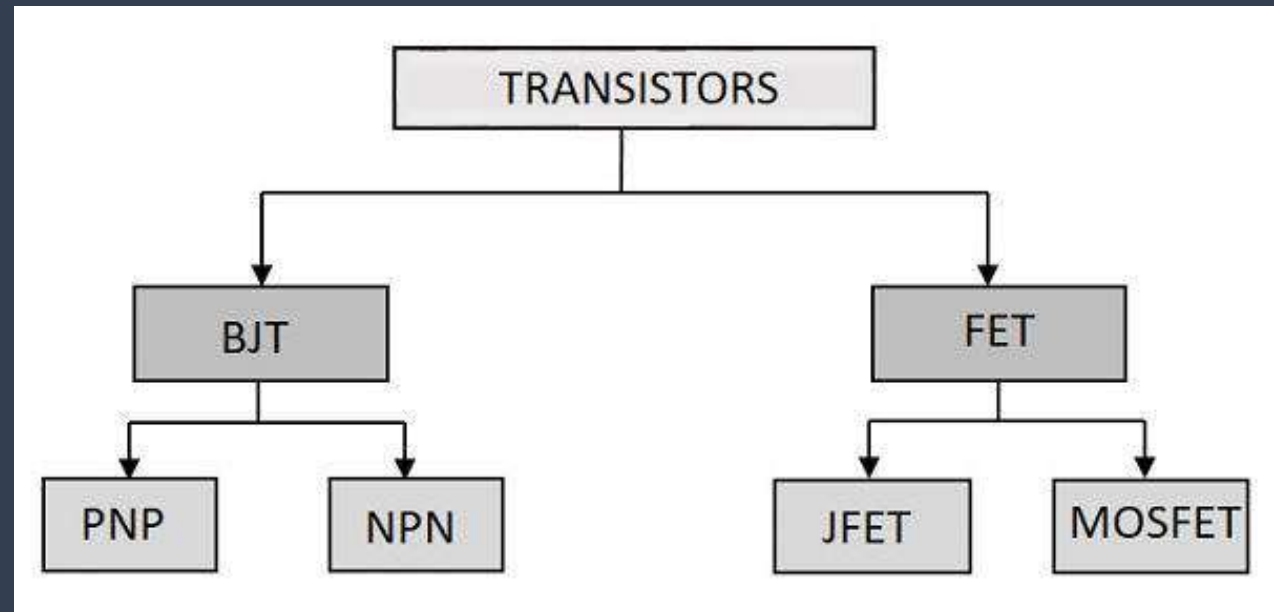
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What is FET ??

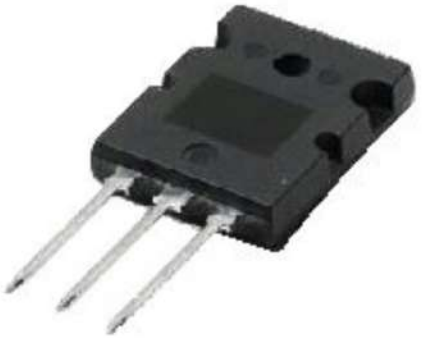
Transistors are two types

1. Bipolar Junction Transistor
2. Field Effect Teansistor

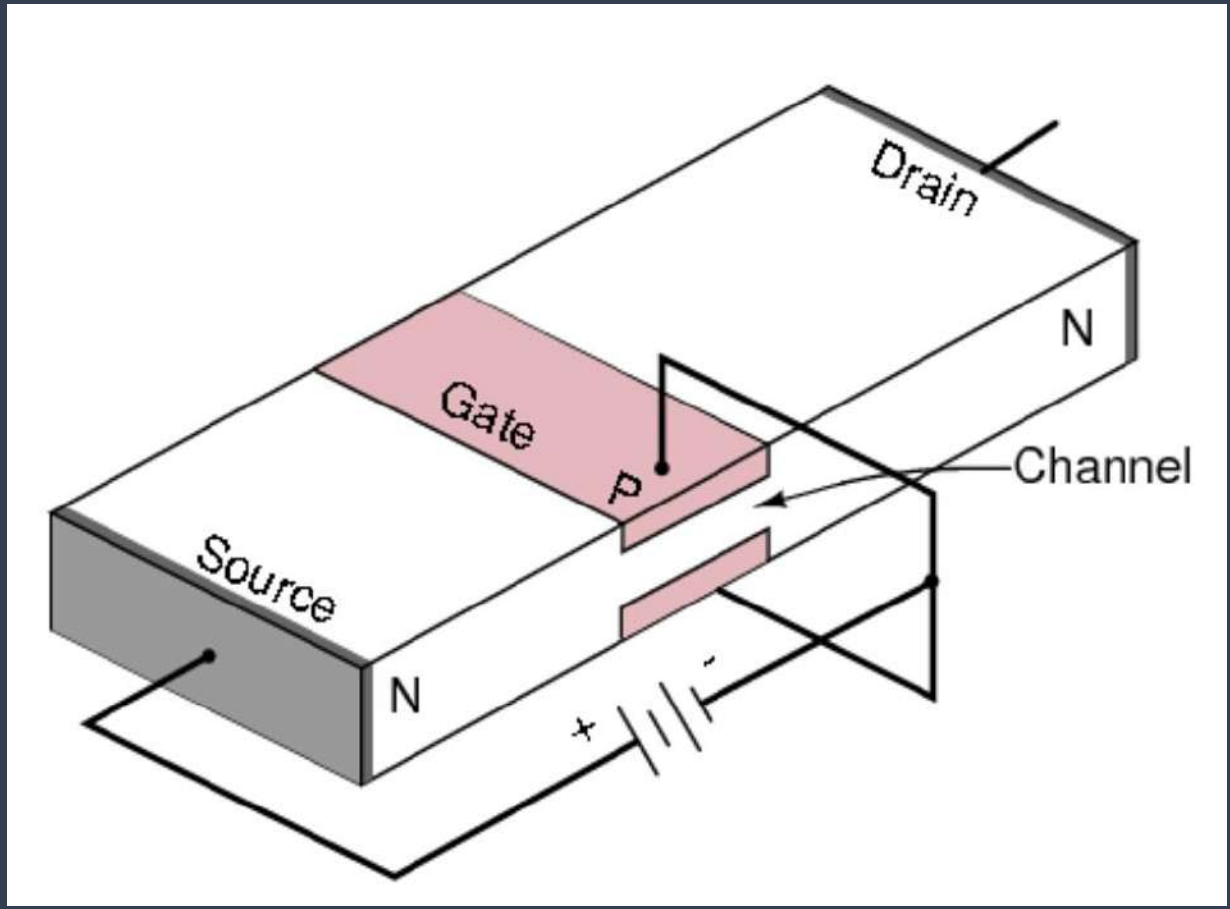


The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the **Gate** to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input **Gate** voltage, this then makes the **Field Effect Transistor** a “**VOLTAGE**” operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.



Typical Field Effect Transistor



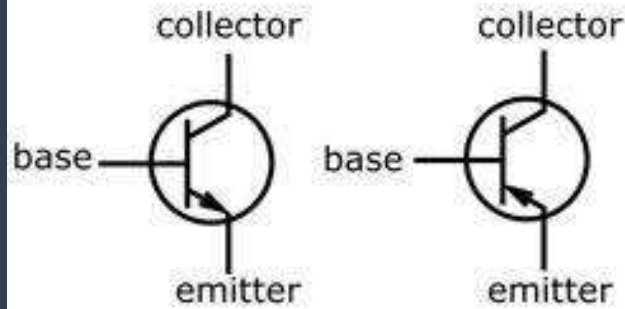
Comparison of BJT and FET

All field-effect transistors are unipolar rather than bipolar devices. That is, the main current through them is comprised either of electrons through an N-type semiconductor or holes through a P-type semiconductor. This becomes more evident when a physical diagram of the device is seen:

The **Field Effect Transistor** has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (R_{in}) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

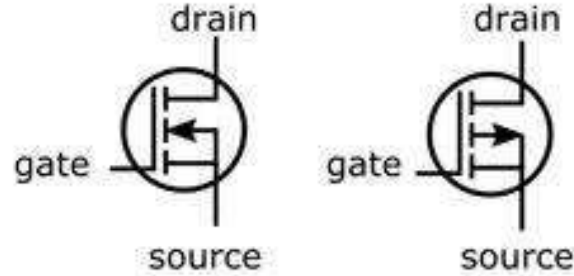
bipolar junction transistors (BJTs)

field-effect transistors (FETs)



NPN

PNP



N-channel
MOSFET

P-channel
MOSFET

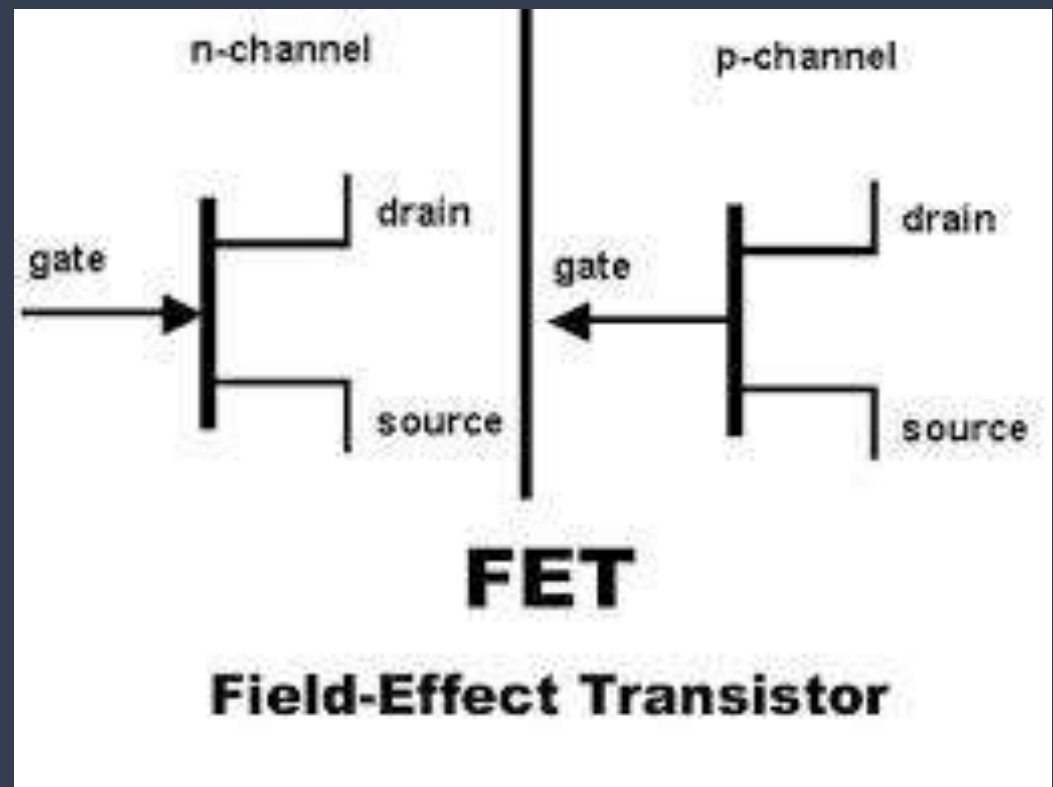
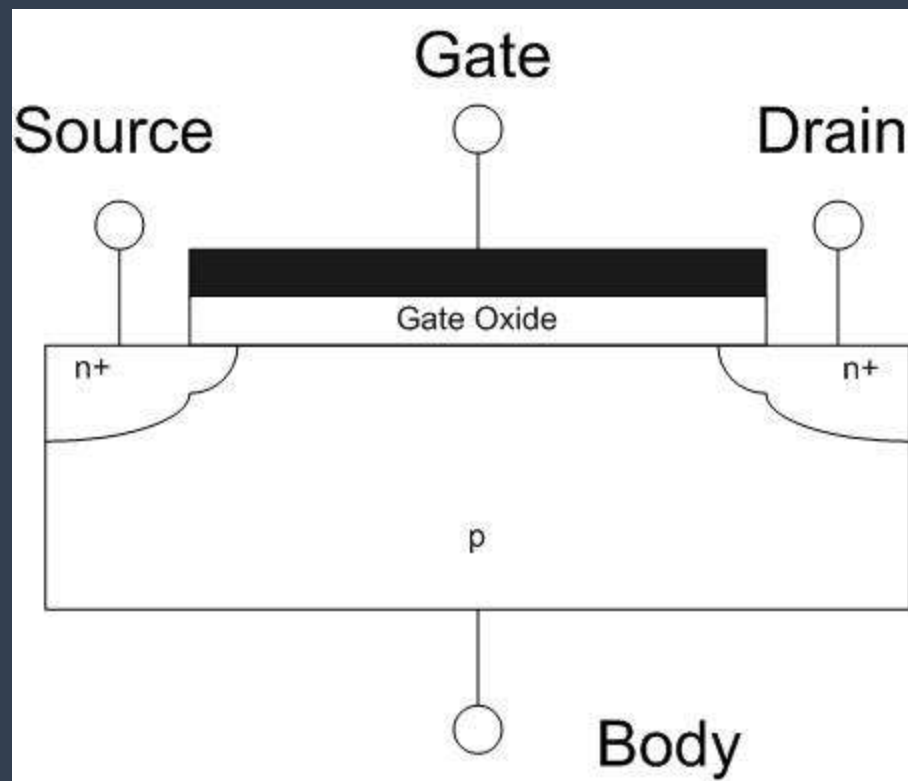
We remember from the previous tutorials that there are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. This is also true of FET's as there are also two basic classifications of Field Effect Transistor, called the N-channel FET and the P-channel FET.

The following notations are used for the FET.

Source (S): The terminal through which the majority carriers enter the bar is known as the *source*.

Drain (D): The terminal through which the majority carriers leave the bar is referred to as the *drain*.

Gate (G): The regions on the two sides of the bar heavily doped with impurities opposite to that of the bar, are called the *gate*.



Clear your idea more

<https://youtu.be/g4nBAifUVik>

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Junction Field Effect Transistor

The JFET

This was the earliest FET device available. It is a voltage-controlled device in which current flows from the SOURCE terminal (equivalent to the emitter in a bipolar transistor) to the DRAIN (equivalent to the collector). A voltage applied between the source terminal and a GATE terminal (equivalent to the base) is used to control the source - drain current. The main difference between a JFET and a bipolar transistor is that in a JFET no gate current flows, the current through the device is controlled by an electric field, hence "Field effect transistor". The

Characteristics of JFET for being commonly used:

- Fast switching
- For low frequency operation, source and drain can be interchanged
- Gate voltage that controls drain current
- Single majority carrier
- Small in size
- High "Z" input

The JFET

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JFET Construction

The construction of JFETs can be theoretically quite simple, but in reality difficult, requiring very pure materials and clean room techniques. JFETs are made in different forms, some being made as discrete (single) components and others, using [planar technology](#) as integrated circuits.

Fig.1.1 Diffusion JFET Construction

Fig. 1.1 shows the (theoretically) simplest form of construction for a Junction FET (JFET) using diffusion techniques. It uses a small slab of N type semiconductor into which are infused two P type areas to form the Gate. Current in the form of electrons flows through the device from source to drain along the N type silicon channel. As only one type of charge carrier (electrons) carry current in N channel JFETs, these transistors are also called "Unipolar" devices.

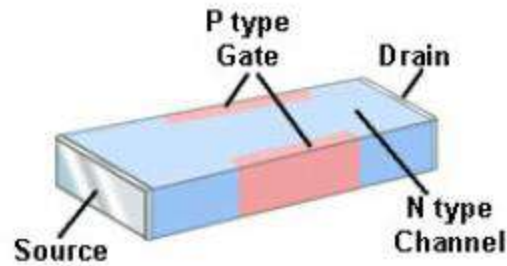


Fig. 1.3 JFET Circuit symbols

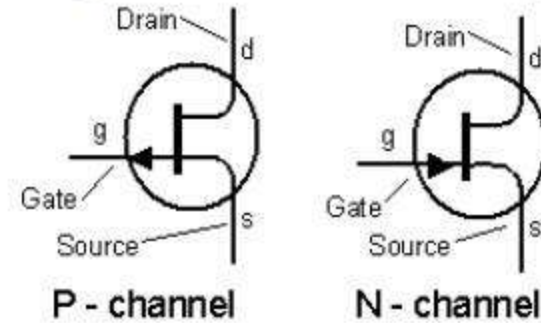
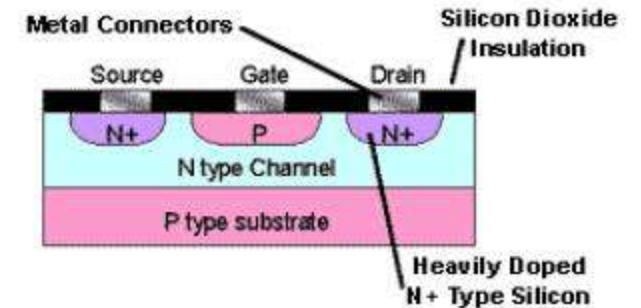


Fig. 1.2 JFET Planar Construction

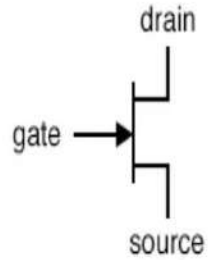
Fig. 1.2 shows the cross section of a N channel planar Junction FET (JFET). The load current flows through the device from source to drain along a channel made of N type silicon. In the planar device the second part of the gate is formed by the P type substrate.



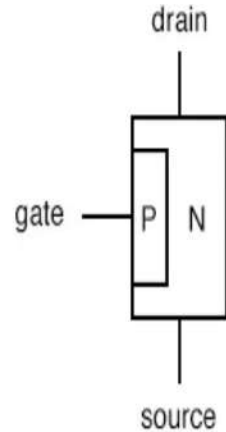
P channel JFETs are also available and the principle of operation is the same as the N channel type described here, but polarities of the voltages are of course reversed, and the charge carriers are holes.

N-channel JFET

N-channel JFET



schematic symbol

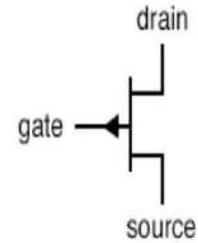


physical diagram

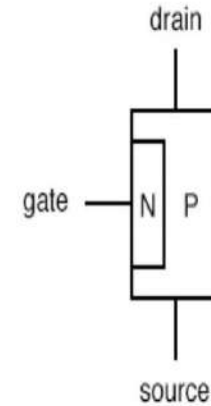
In a **junction field-effect transistor** or JFET, the controlled current passes from source to drain, or from drain to source as the case may be. The controlling voltage is applied between the gate and source. Note how the current does not have to cross through a PN junction on its way between source and drain: the path (called a channel) is an uninterrupted block of semiconductor material. In the image just shown, this channel is an N-type semiconductor. P-type channel JFETs are also manufactured:

P-channel JFET

P-channel JFET



schematic symbol



physical diagram

Generally, N-channel JFETs are more commonly used than P-channel. The reasons for this have to do with obscure details of semiconductor theory, which I'd rather not discuss in this chapter. As with **bipolar transistors**, I believe the best way to introduce field-effect transistor usage is to avoid theory whenever possible and concentrate instead on operational characteristics. The only practical difference between N- and P-channel JFETs you need to concern yourself with now is biasing of the PN junction formed between the gate material and the channel.

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Characteristics of JFET

13.3 STATIC CHARACTERISTICS OF JFET

The graphical plots of the drain current (I_D) against the drain-to-source voltage (V_{DS}) with the gate-to-source voltage (V_{GS}) as a parameter are known as the *static* or the *common-source drain characteristics of a JFET*. The typical static characteristics of an *n*-channel JFET are depicted in Fig. 13.4.

The drain characteristics are found to consist of three regions (i) the *linear* or *ohmic region*, where the voltage V_{DS} is small and I_D is nearly proportional to V_{DS} ; (ii) the *saturation region*, where I_D is fairly constant and is independent of V_{DS} ; and (iii) the *breakdown region*, where I_D increases rapidly with a small increase of V_{DS} .

The constant drain current in the saturation region of the characteristics is called the *saturation current*, I_{Dsat} . The minimum value of V_{DS} at which the drain current saturates for a given V_{GS} is called the *saturation voltage*, V_{DSat} . As the reverse gate bias increases, both I_{Dsat} and V_{DSat} diminish. The points of intersection of the dashed curve with the characteristics give the values of I_{Dsat} and V_{DSat} for different V_{GS} .

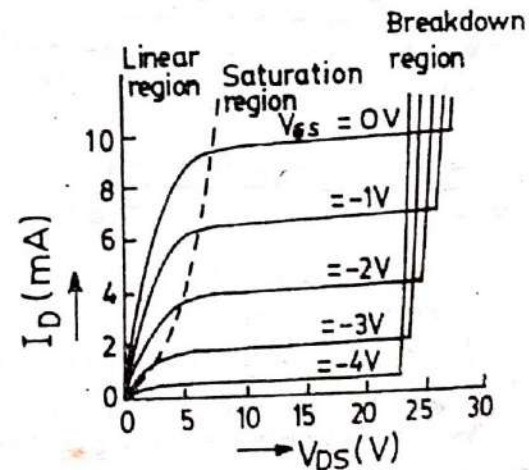


Fig. 13.4 Static characteristics of an *n*-channel JFET

The experimental arrangement for obtaining the static characteristics of an n -channel JFET is shown in Fig. 13.5. The voltmeters V_1 and V_2 measure the voltage V_{DS} and V_{GS} , respectively. The drain current I_D is recorded by the milliammeter mA .

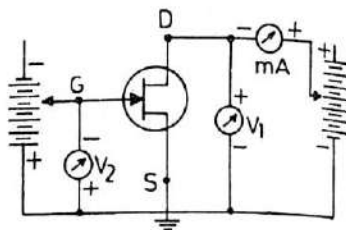


Fig. 13.5 Experimental arrangement for obtaining the drain characteristics of an n -channel JFET

Explanation of the static characteristics: We consider that $V_{GS} = 0$. When a positive voltage V_{DS} is applied to the drain with respect to the source, the voltage V_x increases along the channel from zero at the source to V_{DS} at the drain. As V_{DS} increases from zero to a small value, the widths of the depletion regions remain very small and the semiconductor bar behaves as a simple resistor. Therefore, the drain current I_D increases linearly with V_{DS} . This accounts for the *linear region* of the characteristic.

The reverse bias across each point in the gate-to-channel junction is V_x when $V_{GS} = 0$. Hence the reverse bias is relatively large near the drain and decreases gradually towards the source. Consequently, the depletion region intrudes into the channel more towards the drain, as shown in Fig. 13.1. As V_{DS} is slowly increased, the depletion layer widths increase thereby constricting the channel opening. The channel resistance thus increases and the drain current rises less than linearly with V_{DS} . As V_{DS} continues to increase, the channel opening near the drain shrinks and the channel resistance increases further. At some value of V_{DS} , the depletion regions meet near the drain to *pinch off* the channel [Fig. 13.6(a)]. This value of V_{DS} is the saturation voltage V_{DSsat} . Beyond pinch-off, the current I_D saturates at a value I_{Dsat} . The differential channel resistance dV_{DS}/dI_D is very high in the *saturation region*.

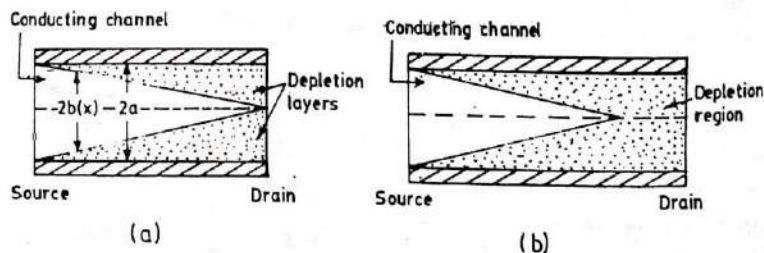


Fig 13.6 Cross-sectional view of a JFET (a) at pinch-off (b) beyond pinch-off

As V_{DS} increases above V_{DSsat} , the excess voltage is absorbed by the depletion regions. Thus the depletion regions meet at a point before the drain end [Fig. 13.6 (b)]. In principle, the channel cannot close completely, for that would force the drain current to zero. The channel becomes very narrow from the point where

the depletion regions *nearly* meet, up to drain. The depletion area widens and the effective channel resistance increases to keep the drain current nearly constant.

For a large value of V_{DS} , the reverse voltage between the channel and the gate becomes sufficient to cause a breakdown of the gate junction, resulting in a sharp increase of the drain current. The *breakdown regions* of the characteristic is thus explained.

When V_{GS} is negative, the channel resistance increases because reverse bias between the channel and the gate is enhanced. Hence the drain current for a given V_{DS} is reduced and the pinch-off occurs at a lower value of V_{DS} . Therefore, V_{DSat} decreases with increasing negative gate voltage. The saturated drain current I_{Dsat} is also lowered by the negative gate-source voltage. Breakdown also takes place at a lower value of V_{DS} as the reverse gate bias increases, because both V_{DS} and V_{GS} contribute to the breakdown voltage.

Note that beyond pinch-off, the drain current is controlled by the gate bias. So, by varying the gate bias, the *amplification* of an ac signal can be achieved.

A forward bias is not applied to the gate because that would cause hole injection from the gate into the channel. The field-effect control of the device is lost and the input impedance is reduced.

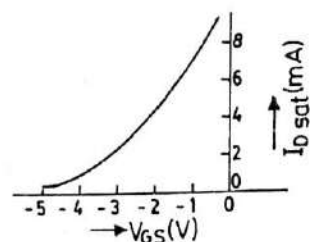


Fig. 13.7 Transfer characteristic of an n -channel JFET

Transfer characteristic of JFET: The graph showing the variation of the saturation drain current I_{Dsat} with gate-to-source voltage V_{GS} is referred to as the *transfer characteristic* of the JFET. The transfer characteristic can be easily obtained from the static characteristics. For an n -channel JFET, the transfer characteristic is shown in Fig. 13.7.

Observation

Figure 13.6 shows a simplified picture at and beyond pinch-off. A more realistic cross-sectional view of a JFET before, at, and beyond pinch-off is depicted in Fig. 13.7A.

13.4 PINCH-OFF VOLTAGE

In the n -channel JFET of Fig 13.1, there are two sets of depletion regions, one on each side (upper and lower) of the n -type bar. The two sets are alike, and we consider only one set here. Let W_n be the width of the depletion region in the n -type bar and W_p be that in the p -type gate at a distance x from the source end. If N_A is the concentration of acceptor ions in the p -type gate and N_D is that of the donor ions in the n -type bar, we have $N_A W_p = N_D W_n$, because the net charge is zero. The gate being heavily doped, $N_A \gg N_D$. Hence $W_p \ll W_n$, and the net

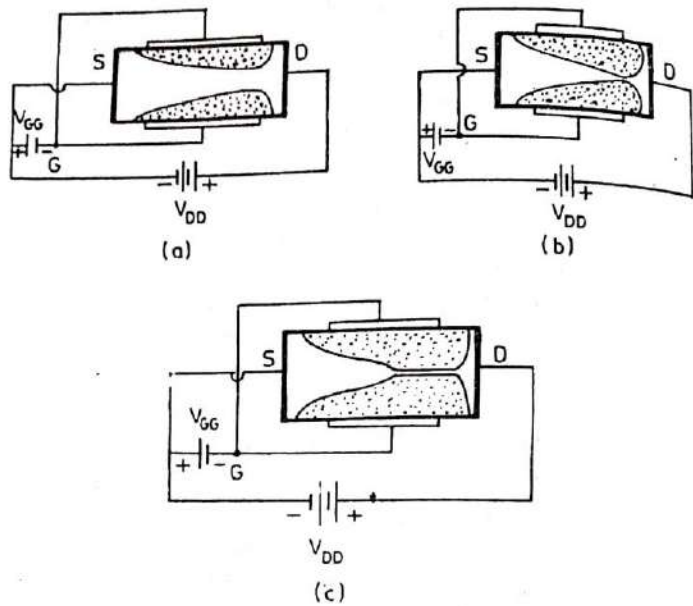


Fig. 13.7A. Realistic picture of an n -channel JFET (a) before pinch-off, (b) at pinch-off, and (c) after pinch-off

width of the depletion region is $W = W_p + W_n \approx W_n$. There being two sets of depletion regions, W is actually the depletion-layer half width. Moving perpendicular to the x -direction, i.e. along the y -direction, Poisson's equation for the depletion region in the n -type bar is (in SI units)

$$\frac{d^2V}{dy^2} = -\frac{e}{\epsilon} N_D,$$

where e is the magnitude of the electronic charge and ϵ is the permittivity of the material of the bar. The boundary condition is that at $y = W_n = W$, the barrier electric field $F = -\frac{dV}{dy} = 0$. Integrating the above equation and using the boundary condition, we obtain

$$\frac{dV}{dy} = -\frac{e N_D}{\epsilon} (y - W) = -F.$$

Again integrating, we get

$$\int_0^y dV = -\frac{e N_D}{\epsilon} \int_0^y (y - W) dy$$

or,

$$V(y) = -\frac{e N_D}{2\epsilon} (y^2 - 2Wy).$$

At $y = W$, we have $V(y) = IV(x)$, which is the applied voltage across the space-charge region at x . We have neglected here the built-in potential between the channel-gate junction. $V(x)$ is negative because of reverse bias for an n -channel JFET. If a is the half-width of the bar and $b(x)$ is the half-width of the conducting channel [Fig. 13.6(a)], the depletion-layer half-width at x can be obtained from the last equation by putting $y = W(x)$. Thus

$$W(x) = a - b(x) = \left[\frac{2\epsilon}{e N_D} |V(x)| \right]^{1/2} \quad (13.1)$$

Writing $C = e N_D / (2\epsilon)$, Eq. (13.1) can be put in the form

$$|V(x)| = C [a - b(x)]^2 \quad (13.2)$$

The magnitude of the voltage across the space-charge region for which the channel is just pinched off near the drain is called the *pinch-off voltage*, denoted by V_p . V_p is a positive number and is related to V_{DSAT} and V_{GS} by

$$V_p = V_{DSAT} - V_{GS} \quad (13.3)$$

where V_{GS} is zero or negative. Clearly, the value of V_{DSAT} obtained from the static characteristics for $V_{GS} = 0$, gives the pinch-off voltage V_p . The saturation drain current for $V_{GS} = 0$ is known as the *pinch-off current*, I_p .

Equation (13.3) shows that pinch-off takes place from a combination of gate-to-source voltage and drain-to-source voltage. Pinch-off is reached at a lower value of V_{DSAT} when a negative gate bias is applied.

At pinch-off, $b(x) = 0$ at the drain end [see Fig. 13.6 (a)]. Therefore, Eq. (13.2) gives for the pinch-off voltage

$$V_p = C a^2 = \frac{e N_D}{2\epsilon} a^2 \quad (13.4)$$

For a p -channel JFET, N_D in Eq. (13.4) should be replaced by N_A , the acceptor concentration in the channel bar.

If $b(x)$ decreases almost linearly with x , such that $b(x) = a - kx$ (where k is a constant), we obtain from Eqs. (13.2) and (13.4)

$$|V(x)| = V_p \left[1 - \frac{b(x)}{a} \right]^2 = V_p \frac{k^2 x^2}{a^2} \quad (13.5)$$

Noise behaviour: JFETs are useful for low-noise amplification. The noise is less because only the majority carriers participate in the device operation. In practical devices, however, the thermal noise in the resistances contributes to the noise behaviour. For low-noise performances, the gate length and channel width must be reduced. Unlike the BJT, the noise figure of FETs is independent of the quiescent point (I_D and V_{DS}).

What is Pinch off Voltage

Pinch off voltage is the drain to source voltage after which the drain to source current becomes almost constant and JFET enters into saturation region and is defined only when gate to source voltage is zero.

<https://youtu.be/-o39YVNMYYVs>

Solved Problems

2. The Q -point of a JFET in a source self-bias arrangement is chosen at $V_{GS} = -1.5$ V and $I_{Dsat} = 5$ mA. Find the value of the resistance R_s .

Ans. We have

$$R_s = \frac{|V_{GS}|}{|I_{Dsat}|} = \frac{1.5}{5 \times 10^{-3}} \text{ ohm} \\ = 300 \text{ ohm.}$$

3. As V_{GS} is changed from -1 V to -1.5 V keeping V_{DS} constant, I_D of a FET drops from 7 to 5 mA. What is the transconductance of the FET? If the ac drain resistance is 200 kilo ohm, find also the amplification factor of the FET.

Ans. The transconductance is

$$g_m = \left. \frac{i_d}{v_{gs}} \right|_{V_{DS}} = \frac{7 - 5}{-1 - (-1.5)} \frac{\text{mA}}{\text{V}} \\ = 4 \text{ mA/V}$$

The amplification factor is

$$\mu = r_d g_m = 200 \times 10^3 \times 4 \times 10^{-3} = 800.$$

4. A FET amplifier in the common-source configuration uses a load resistance of 250 k Ω . The ac drain resistance of the device is 100 k Ω and the transconductance is 0.5 mA/V. What is the voltage gain of the amplifier?

Ans. The voltage gain is

$$A_v = - \frac{\mu R_L}{r_d + R_L}$$

Here $r_d = 100$ kilo ohm, $g_m = 0.5$ mA/V, and $R_L = 250$ kilo ohm. We have $\mu = r_d g_m = 100 \times 0.5 = 50$. Hence

$$A_v = - \frac{50 \times 250}{100 + 250} = - 35.71$$

Assignment

2. An n -channel JFET gives a saturation voltage $V_{Dsat} = 4V$ for $V_{GS} = -1V$. Another n -channel JFET gives $V_{Dsat} = 6.5V$ for the same V_{GS} . Compare the pinch-off voltages of the two JFETs. (Ans. 2:3)
3. For a constant V_{GS} , the drain current of a FET changes by $20 \mu A$ when V_{DS} is changed by $2V$. What is the ac drain resistance? (Ans $100 k\Omega$)
4. The transconductance and the ac drain resistance of a FET are $0.2 mA/V$ and $150 k\Omega$, respectively. This device is used in the CS configuration with a load resistance of $150 k\Omega$. Determine the small-signal voltage gain (Ans. -15)

